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Gate oxice leakage in poly-depleted nanoscale-MOSFET: a quantum mechanical study

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Abstract

In this paper, we investigate the effect of depletion and doping variation in the poly-silicon on the direct tunneling current of an ultra thin oxide n-MOSFET. The one dimension (1-D) poly silicon depletion effect has been analytically modeled. The tunneling probability is calculated by Wentzel–Kramers–Brilliouin (WKB) approximation. The results show a decrease in tunneling current density under poly depletion conditions and increase if the doping density in the poly increases. The results have also been compared with the numerically reported results which show good agreement.

Keywords: Quantization; Tunneling; Model.
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1. Introduction

The MOSFETs have scaled down aggressively over the years since their invention. This has resulted in accommodating more MOSFETs on the same actual layout area and has also resulted in the increased performance. The scaling has hence resulted in cutting the manufacturing cost per transistor and yielded enhanced profits [1]. With continuous scaling of gate dielectrics with technology scaling to nanoscale dimensions, an accurate direct tunneling modeling is critical and necessary to understand the scaling limits. Aggressive scaling of CMOS technology in recent years has reduced the silicon dioxide gate dielectric thickness of about 2nm or below. Major causes for concern in further reduction of the SiO2 thickness include increased poly-silicon gate depletion, gate dopant penetration into the channel, high direct tunneling induced gate leakage current, reliability issues, and stand-by power consumption. The increased leakage is a well-recognized challenge for further MOSFET scaling. When bulk CMOS technology evolves from one generation to the next, the channel doping concentration is increased and the gate oxide thickness is reduced to mitigate sub threshold leakage currents and manage short channel effects [2]. This process of scaling CMOS has worked well for over the last several decades. For gate lengths below 90 nm, the gate oxide thickness is estimated to be less than 2nm [3]. Current device scaling requires 1 nm thin oxide film within the next 10 years. In a MOSFET with such ultra-thin

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oxides, the direct tunneling current is expected to contribute significantly to the leakage current [4]. Furthermore, the decrease in the channel current due to the oxide leakage results in low drain currents and hence the operation of circuits at low power is seriously hampered. For oxide films with thickness less than 2.0 nm, the tunneling current will increase exponentially leading to increased power dissipation. Furthermore, it is predicted that the oxide layer with thickness less than 1.0 nm would be too thin for showing any resistance to electron tunneling. The paper is organized as follows: The paper starts with the modeling of inversion layer quantization. Secondly, poly depletion modeling has been done. Lastly, direct tunneling model based on WKB approximation has been used to calculate the gate leakage current for SiO2 considering poly silicon depletion and effect of variation in doping concentration in polysilicon has been studied.

2. Inversion Layer Quantization

The research in the area of energy quantization started in the early 1950s. The research[5]-[9] mainly focused on only calculating the inversion charge density in the presence of energy quantization effects using variation approach and triangular well approach in the MOSFET. The use of such techniques required the calculation of surface potentials at the interface of silicon and its oxide. But as the MOSFETs are being scaled down to the nm scale, there is a need to analytically model the inversion layer quantization in nanoscale MOSFETs. Solving the Poisson equation in the inverted channel, we get the total charge density, Qs.

$$Q_s = -(2qN_a\varepsilon_{si}\varepsilon_0)^{1/2}\left[\varphi_s + V_t e^{-2\varphi_f/V_t}\left(e^{\varphi_s/V_t} - 1\right)\right]^{1/2} \tag{1}$$

q is electron charge, ε_{si} is silicon relative permittivity, ε_0 is permittivity of free space, φ_s is surface potential, φ_f is Fermi potential, Na is substrate concentration, and $V_t = kT/q$ is thermal voltage. Similarly, the depletion charge Qb is approximated from the Poisson equation as:

$$Q_b = -(2e_{si}e_o qN_a\varphi_s)^{1/2} \tag{2}$$

Therefore, the inversion charge density Q_{inv} is given by (1) and (2):

$$Q_{\text{inv}} = -\gamma C_{\text{ox}}\left\{\left[\varphi_s + \frac{kT}{q}\exp\left(\frac{q(\varphi_s - 2\varphi_f)}{kT}\right)\right]^{1/2} - (\varphi_s)^{1/2}\right\} \tag{3}$$

γ is body effect parameter and Cox is oxide capacitance. The main problem with (3) is that the surface-potential has to be evaluated explicitly in all the regions of inversion and then only, equation (3) can be solved. An explicit solution has been evaluated in the reference [10]. The wave function solution of the Schrödinger's equation is given by using variation approach [13]:

$$\psi(x) = \frac{b^{3/2}x}{\sqrt{2}}\exp\left(\frac{-bx}{2}\right) \tag{4}$$

b is a constant and given by $$b = \left[\frac{48\pi^2 m^* q}{\varepsilon_{si}\varepsilon_0 h^2}\left(0.33Q_{\text{inv}} + Q_{\text{dep}}\right)\right]^{1/3}$$

m^* is effective longitudinal mass of electron in (100) crystal orientation = 0.98 m0, .The corresponding shift in the energy [13] is given by

$$E_o = \frac{3h^2 b^2}{8m^*} \tag{5}$$

The shift in the surface potential is $= E_o / q$ (6)

(6) is then included in the explicit surface potential expression given by [10] and the total surface potential is obtained. Then a model of quantum inversion charge density is obtained from (3) by including surface potential from [10]. The results in figure 1 match show a reduction in inversion charge density due to inversion layer quantization effects. The results match quite closely with the BSIM 5 results [11]. It has been analytically proved that the classical theory overestimates the value of inversion layer charge density as compared to the quantum mechanical charge density.

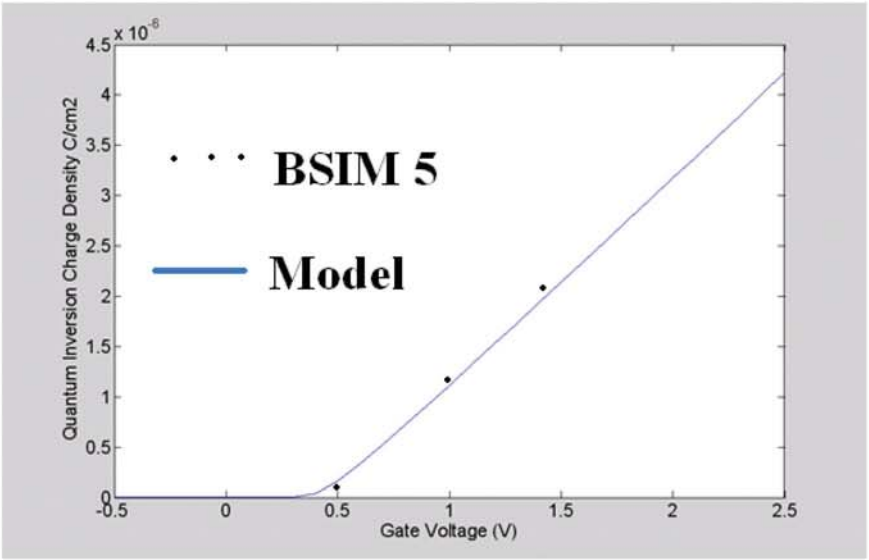

Fig. 1: Simulated results of quantum mechanical inversion charge density with gate voltage under the model parameters: substrate doping 1018cm-3 and oxide thickness 1.5 nm.

3. Poly Silicon Depletion

Poly-silicon gates are used in nanometer MOSFETs instead of metal gates in order to minimize the work function difference in the MOSFET. The poly-silicon gates are of n-type in n-MOSFETs. So, as the gate voltage is increased, the potential drops across the poly-silicon gate also. It causes the charge carriers in the gate to get depleted and exposing the

donor ions. This causes depletion in the gate and this effect is called as poly-silicon gate depletion effect as shown in figure 2. This potential hence, reduces the effective voltage in the oxide and the substrate. The reduced voltage in the substrate causes less inversion charge and ultimately less drain current, which is a big cause of concern for the circuits.

3.1 Modeling Technique

Various models [12-14] have already been reported to estimate the poly silicon gate depletion potential but most of them are either empirical or too complex in modeling procedure. The applied gate to source voltage is distributed across the poly silicon gate, oxide and silicon substrate as shown in figure 3. Applying the voltage equality at the poly silicon gate, we get

$$V_{gs} = V_{ox} + V_{fb} + \varphi_s + V_p \tag{7}$$

Vox= Oxide potential, Vfb= Flat band voltage, φs= Surface potential, Vp= poly silicon gate potential. The poly silicon gate potential is also expressed in terms of polygate electrical field as

$$V_p = X_d E_p \tag{8}$$

Ep =Electric field in the poly silicon gate, Xd =Depletion region in the poly silicon gate.

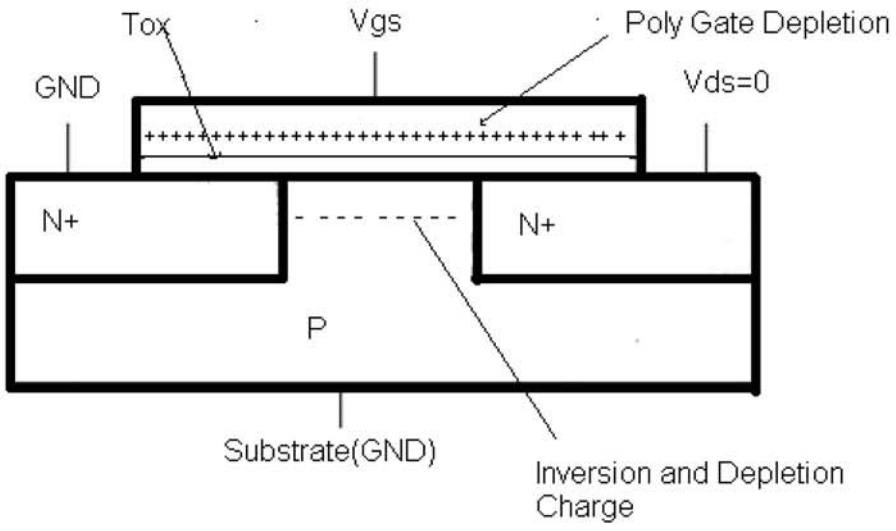

Fig. 2: Poly silicon gate depletion in a MOSFET.

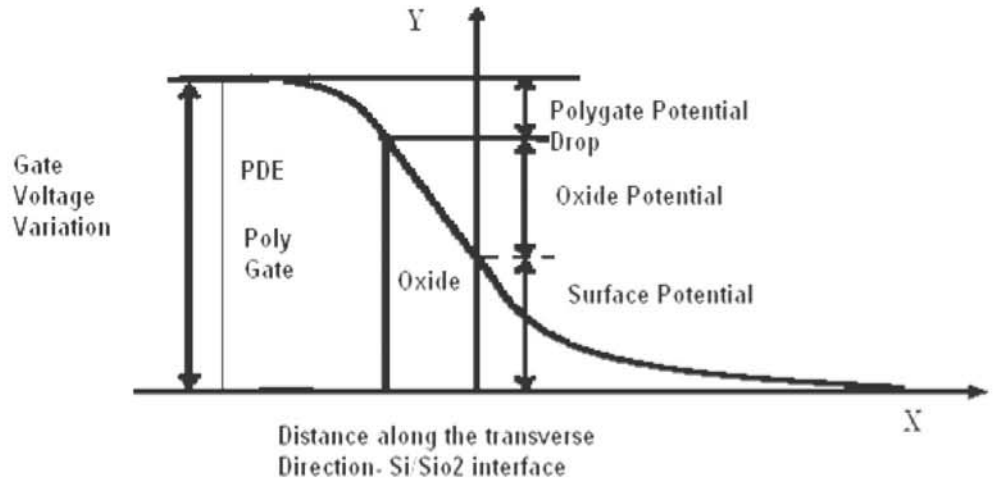

Fig. 3: Variation of potential in the poly silicon gate.

As per the gauss law i.e equating charges at the oxide and substrate interface, we get:

$$e_{si}E_{p} = e_{ox}E_{ox} \tag{9}$$

εsi = Relative permittivity of silicon, εox = Relative permittivity of silicon oxide. From (7-9), we get

$$V_p = X_d (e_{ox} / e_{si})\, E_{ox} \tag{10}$$

Also Oxide electrical field =

$$E_{ox} = V_{ox} t_{ox} \tag{11}$$

And depletion depth in polygate

$$X_d = (2e_o e_p V_p / qN_p)^{1/2} \tag{12}$$

From (9-12), we get

$$V_p = 0.25\left[-\gamma_p + \left\{\gamma_p{}^2 + 4\left(V_{gs} - V_{fb} - \varphi_s\right)\right\}^{1/2}\right]^2 \tag{13}$$

γp =The body coefficient of poly silicon gate = (2qεoεpNp)1/2/Cox. When the poly-depletion effect is accounted for, the potential drop on the gate oxide layer is reduced. Introducing the poly depletion effect in the effective oxide potential, thus changing the barrier height at the oxide /silicon interface, the net effect can be estimated.

4. Theoretical Modeling

An analytical model of gate direct tunneling is used to study electron tunneling directly from the conduction band of the silicon substrate to the conduction band of polysilicon electrode through the SiO2 barrier. The electron concentration at the surface of the Si/Gate-oxide interface and the transmission probability needs to be accurately determined to estimate the gate current. The transmission probability of finding the holes in all the three regions viz. silicon, silicon oxide and the poly silicon can be found from the WKB theory. The tunneling current density can be found by WKB analysis by using the two basic equations i.e. transmission probability and basic tunneling current density [15, 16]:

Transmission probability = $$T(E) = \exp\left[-2\int_{x_1}^{x_2} |k(x)|\,dx\right]$$

k(x) is the wave factor and x1, x2 are the limits of finding the transmission probability and the direct tunneling current density in the gate oxide is given as[5].

$$J_T = \left(\frac{4\pi m^* q}{h^3}\right)\int_0^V \left\{\int_0^\infty \left[f_{Si/SiO2}(E) - f_{Gate}(E)\right]dE_t\right\}T(E_x)dE_x$$

fSi/SiO2(E) = Electron distribution at the Si/SiO2 interface, fGate/Sio2(E)=Electron distribution at the gate/SiO2 interface, m* = 0.19mo for electrons in silicon, Ex=Electron energy in transverse direction, Et= Electron energy in lateral direction, V= Oxide barrier height , mox= 0.61mo for electrons [17].The tunneling is also influenced by the polysilicon depletion which increases the effective oxide thickness and hence reduces the tunneling process. This can be found easily for the various values of 'Vp' and hence the tunneling current density is altered by putting $V_{ox} = V_{gs} - V_{fb} - \varphi_{sQm} - V_p$ in the barrier height V= $q\chi$ - qVox/2, φ_{sQm} is given by [10].

5. Variation In Poly Silicon Gate Doping

The doping concentration of the poly silicon gate has also an effect over the quantum mechanical tunneling current density. The tunneling current density increases as the poly silicon gate doping increases. This is due to the fact that as concentration in the poly silicon gate increases, the depletion in the poly silicon gate will reduce and hence the poly silicon gate depletion effect will decrease.

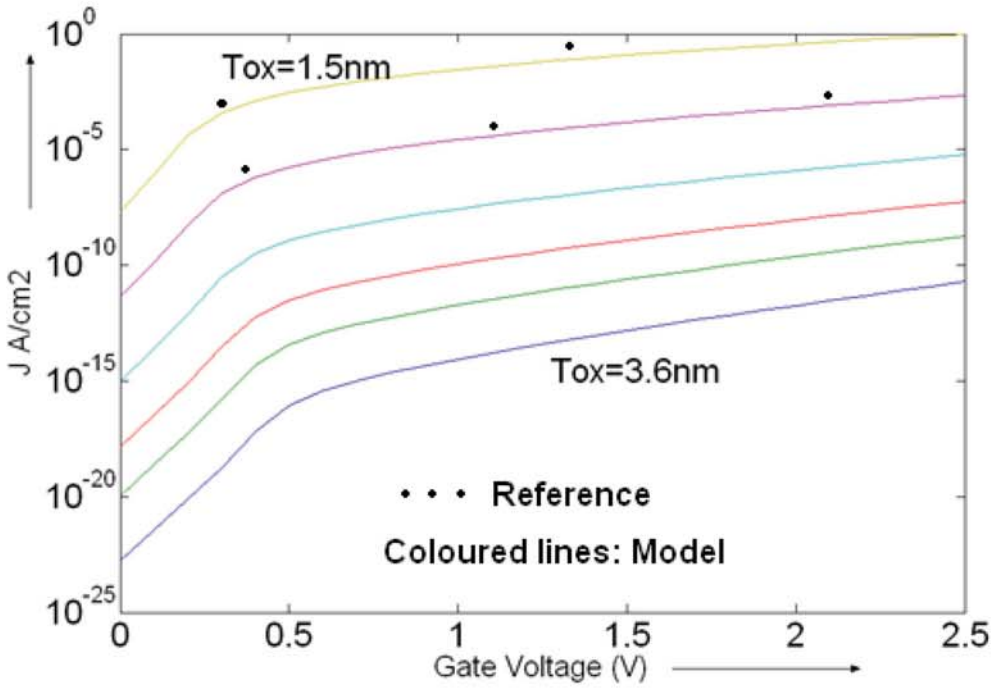

Fig. 4: Poly silicon gate tunneling current density (Acm-2) at various gate to source voltages (Vgs=0-2.5V) and oxide thicknesses (tox=3.6nm-2.0nm-1.5nm) in case of poly silicon gate depletion at the substrate doping of (Nb=5x1017cm-3) and poly silicon gate doping (Np= 5x1019cm-3) at mox=0.61mo.

6. Results and Discussion

Extensive computations have been carried out to estimate the gate electron tunneling currents with the oxide thicknesses from 1.5nm to 3.6nm. The experimental and simulation results [2, 18] predict the tunneling electron current density for poly silicon gate MOSFETs equal to 5x10-4 to 10-1Acm-2 for a 2nm SiO2 at gate voltage from 0-2.5V, substrate doping 1x1017cm-3 and polysilicon doping 1x1019cm-3. The gate electron current without poly depletion is of the order of 10-2 to 10-1Acm-2 and with poly silicon depletion included is of the order of 0 to 10-2Acm-2. The figure 4 clearly indicates a fall in the quantum mechanical tunneling current density due to the effective increase of the oxide thickness in the presence of the poly silicon gate depletion effect. At oxide thickness of 1.5nm, the tunneling current density reduces to one third of the electron tunneling current density value without considering poly silicon depletion effect. As observed in figure 5, at gate voltage of 2.5V and oxide thickness of 2.0 nm, the tunneling current densities increase to a value from 0.1381Acm-2 to 0.1724 Acm-2 as the poly silicon doping concentration increase from 1x1019cm-3 to 1x 1020cm-3. This is due to the reduction in poly silicon gate depletion at higher doping in poly silicon gates which will ultimately decrease the effective oxide thickness. The results are also confirmed with the results mentioned in the reference [19].

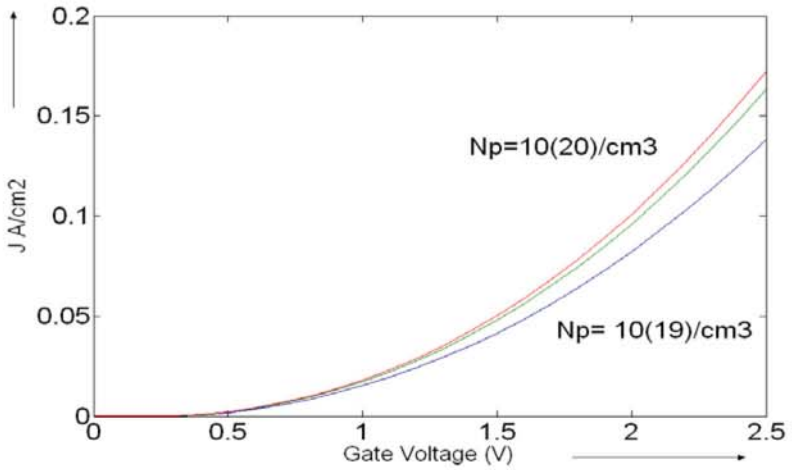

Fig. 5: Variation of tunneling current density with poly silicon gate doping concentration.

7. Conclusion

In this paper, analytical model of direct tunneling for electrons in silicon oxide has been discussed. The consideration of poly depletion and variation of poly doping has a serious effect on the gate oxide leakage. The poly depletion decreases the tunneling and increase of the doping concentration increases the tunneling currents.

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